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Abstract

Method and circuit arrangement for picture-in-picture insertion

The invention relates to a method and a circuit arrangement for picture-in-picture insertion, in which a sequence of insertion pictures (Kj=K1,K2,...) is read, with vertical decimation (VD ≥ 1), into a memory device (S) and subsequently read out, the sequence of insertion pictures (Kj) read out is inserted into a sequence of main pictures (Hi=H1, H2,...) and the memory device (S) is continuously overwritten by the insertion pictures.

In order to prevent the occurrence of a seam during the insertion of the insertion pictures into the main pictures in a cost-effective manner and with a relatively low outlay on apparatus,
the memory device (S) is subdivided into memory segments (X,Y,Z) which are continuously cyclically overwritten by the insertion pictures,
the memory device (S) has a storage capacity of less than two insertion pictures, and
a decision is made as to whether the currently written insertion picture (Kj) or the immediately preceding insertion picture (Kj-1) is read out.

Figure 2